

FIG. 1A (Prior Art)

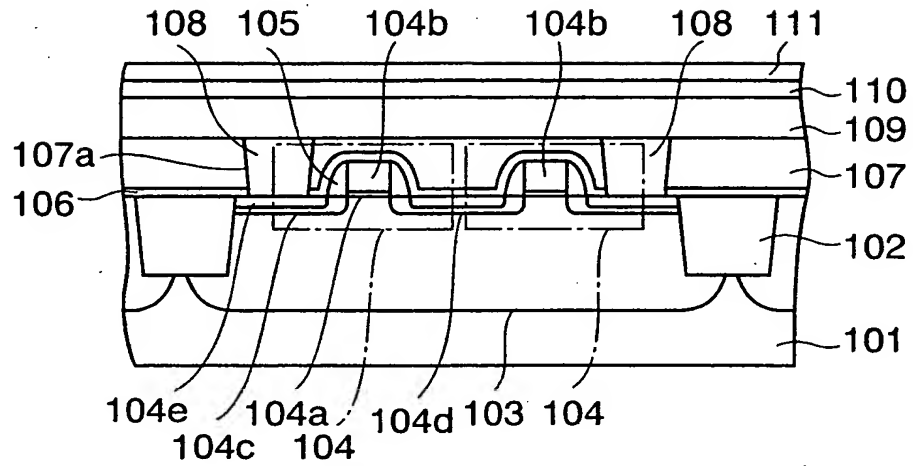
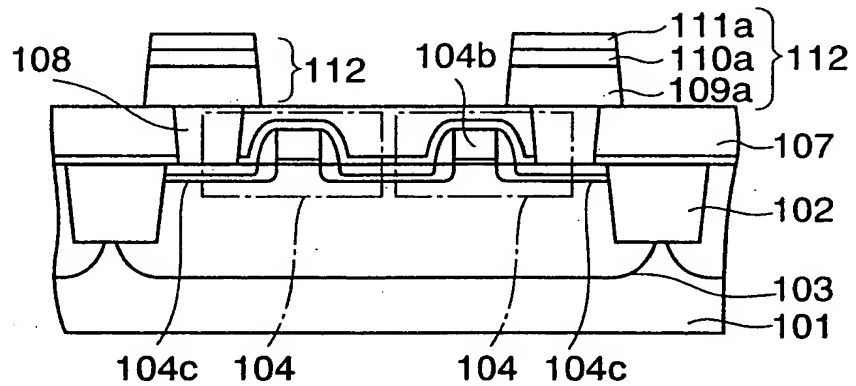


FIG. 1B (Prior Art)



**FIG. 1C (Prior Art)**

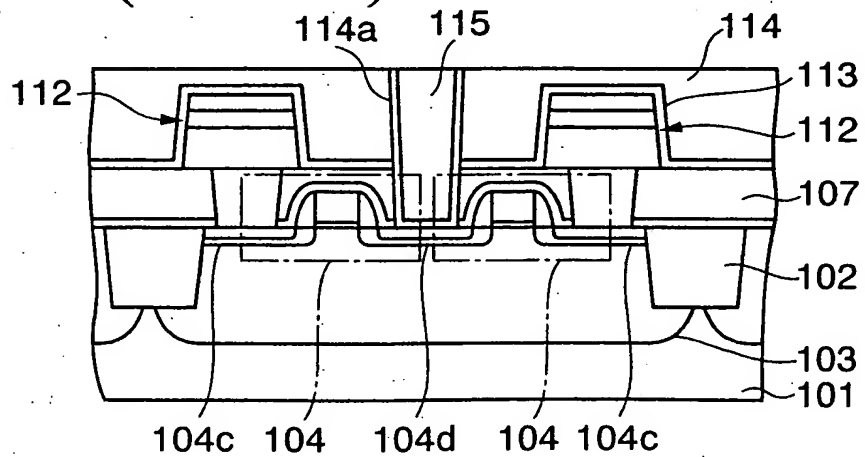


FIG. 1D (Prior Art)

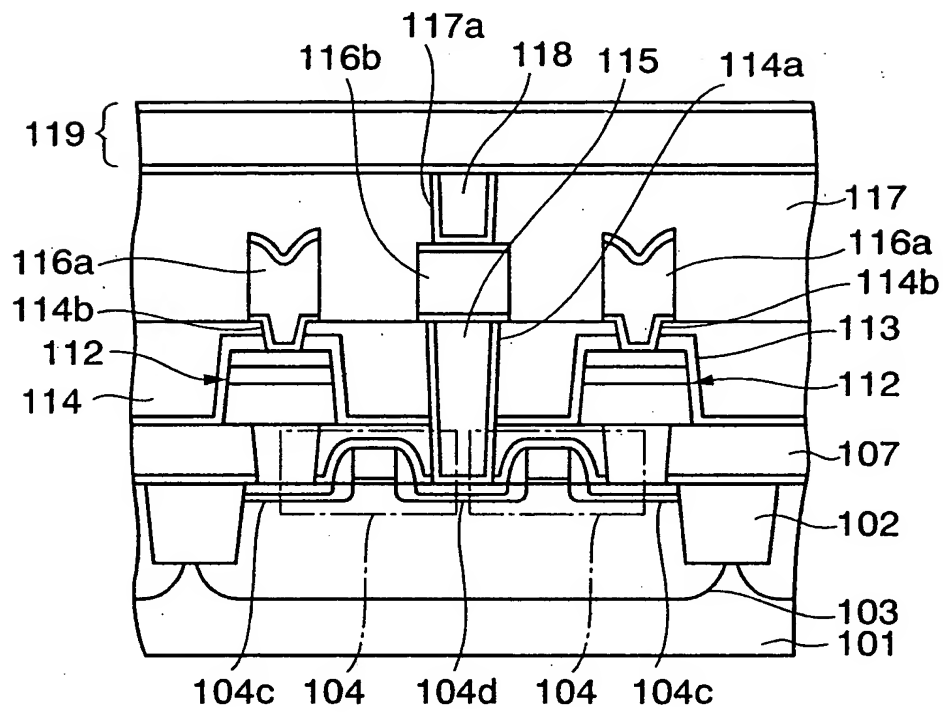


FIG. 2 (Prior Art)

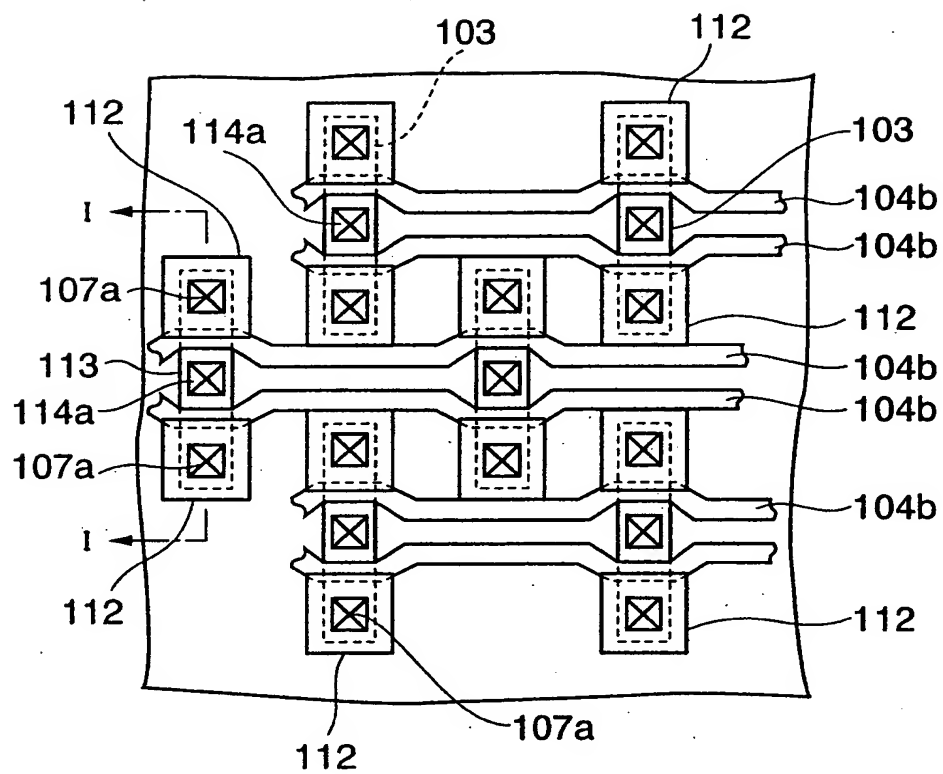


FIG. 3A

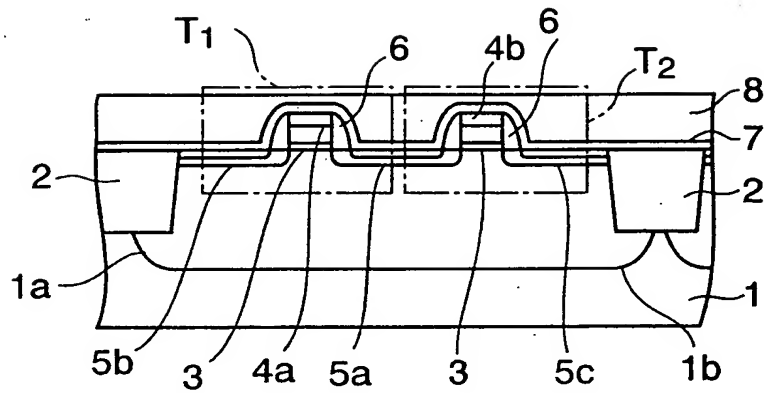


FIG. 3B

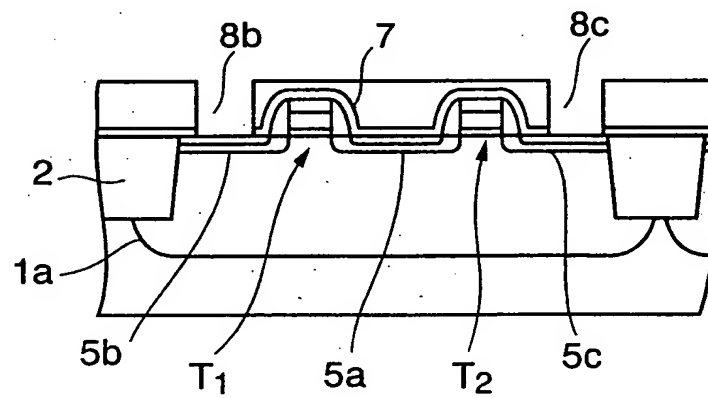


FIG. 3C

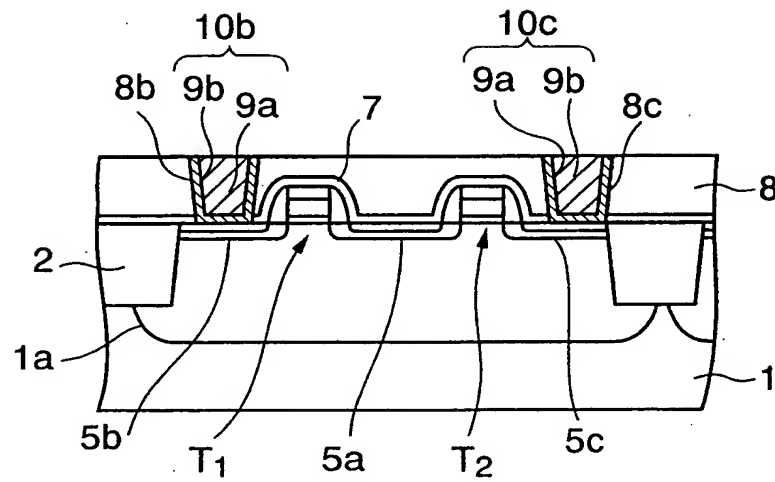


FIG. 3D

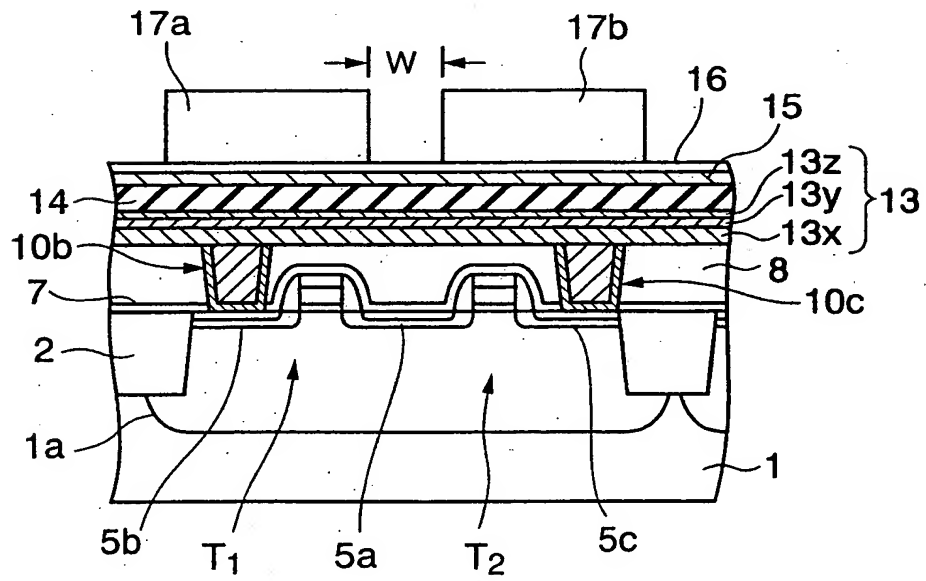


FIG. 3E

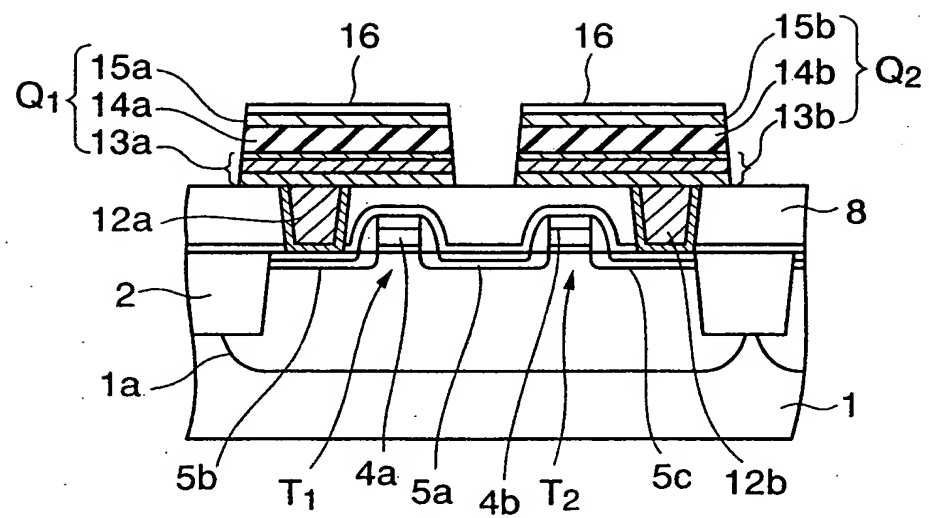
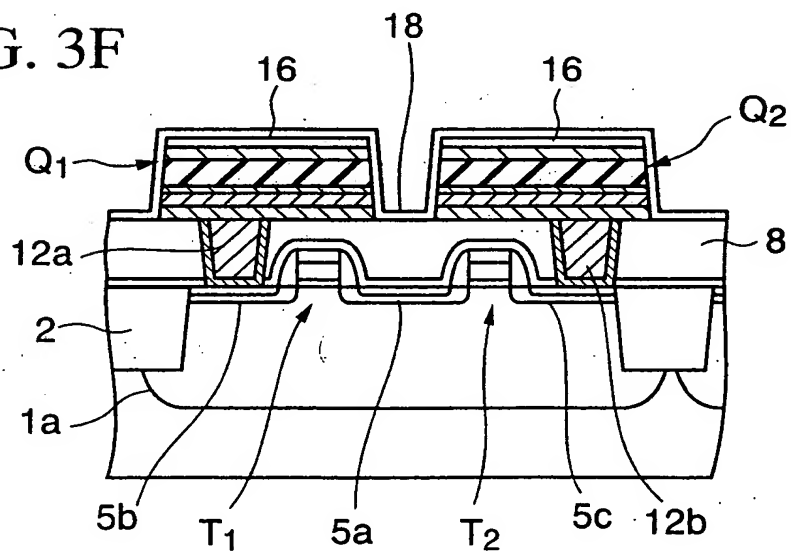


FIG. 3F



A cross-sectional view of a semiconductor device. It shows a substrate with a base layer 1a and a layer 2. Two gates, 5a and 5b, are formed on the surface. Gate 5a is labeled with  $T_1$  and gate 5b with  $T_2$ . The gates are separated by a region 5c. Above the gates are layers 12a and 12b. A layer 7 is located between the gates. A layer 8 is on top of the gates. A layer 18 is on top of the layer 8. A layer 19 is on top of the layer 18. A layer 20 is on top of the layer 19. A layer 16 is on top of the layer 20. A layer 20a is on top of the layer 16. A layer 19a is on top of the layer 19. A layer 18a is on top of the layer 18. A layer 16a is on top of the layer 16a.

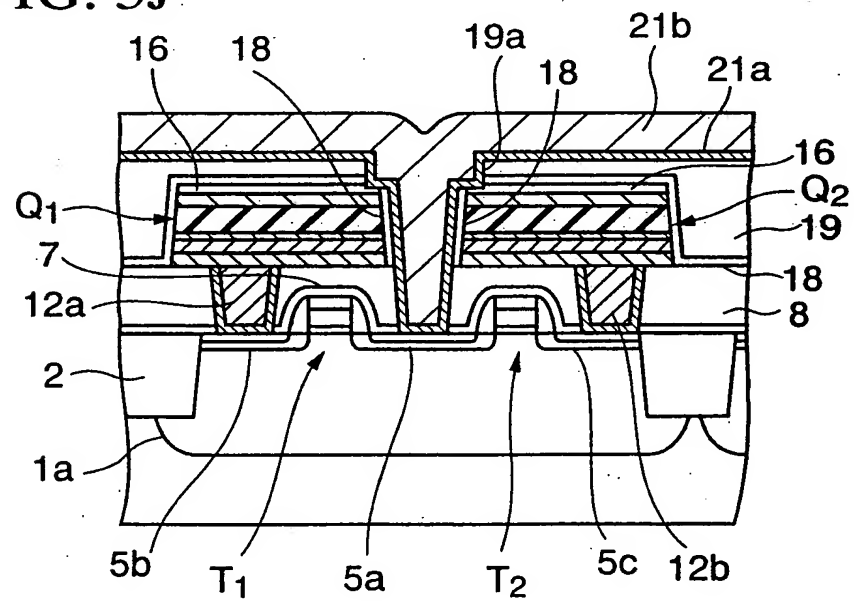




FIG. 3K

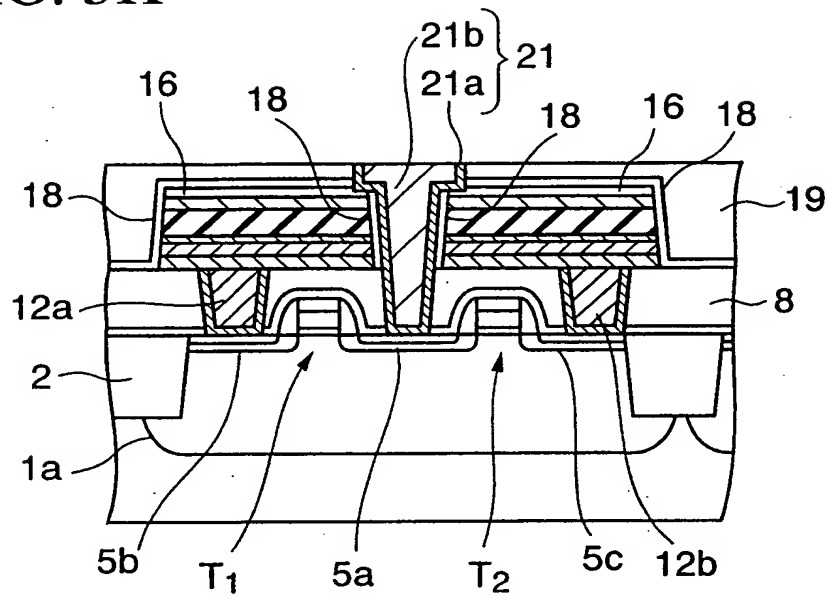


FIG. 3L

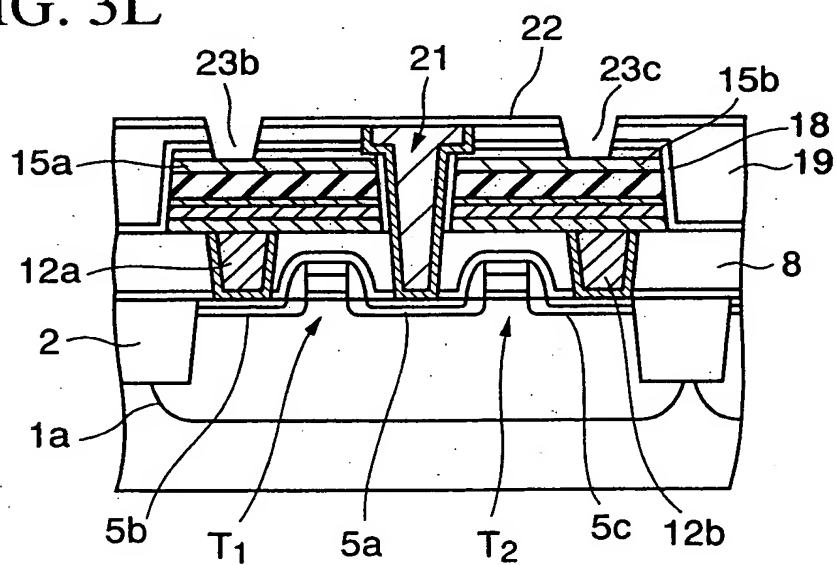


FIG. 3M

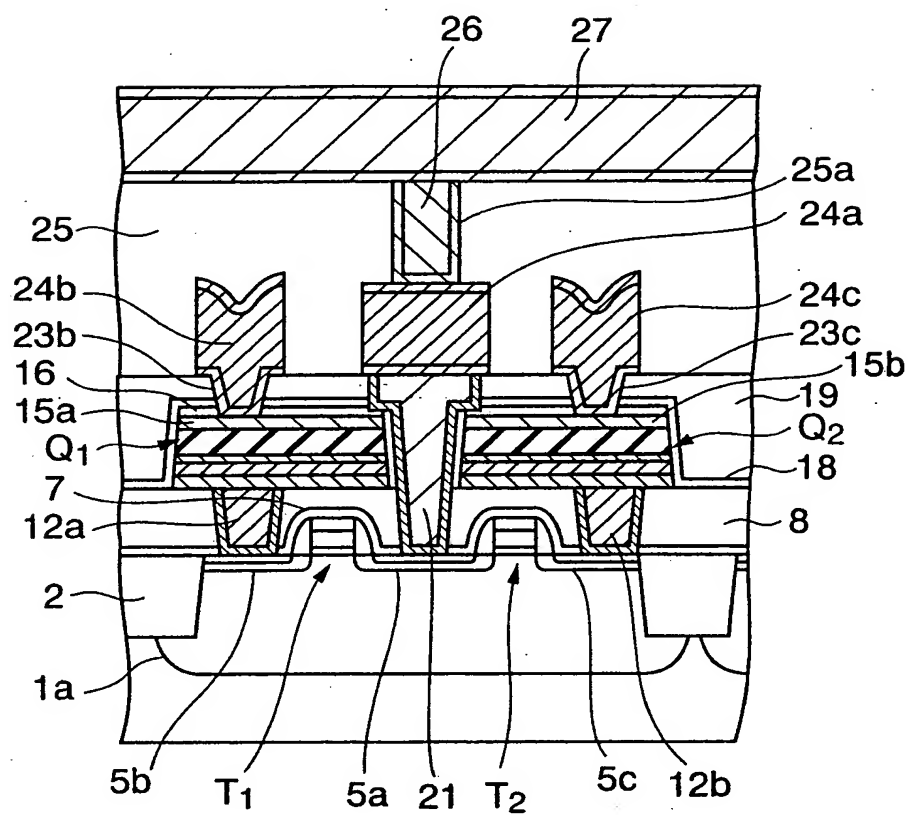


FIG. 4

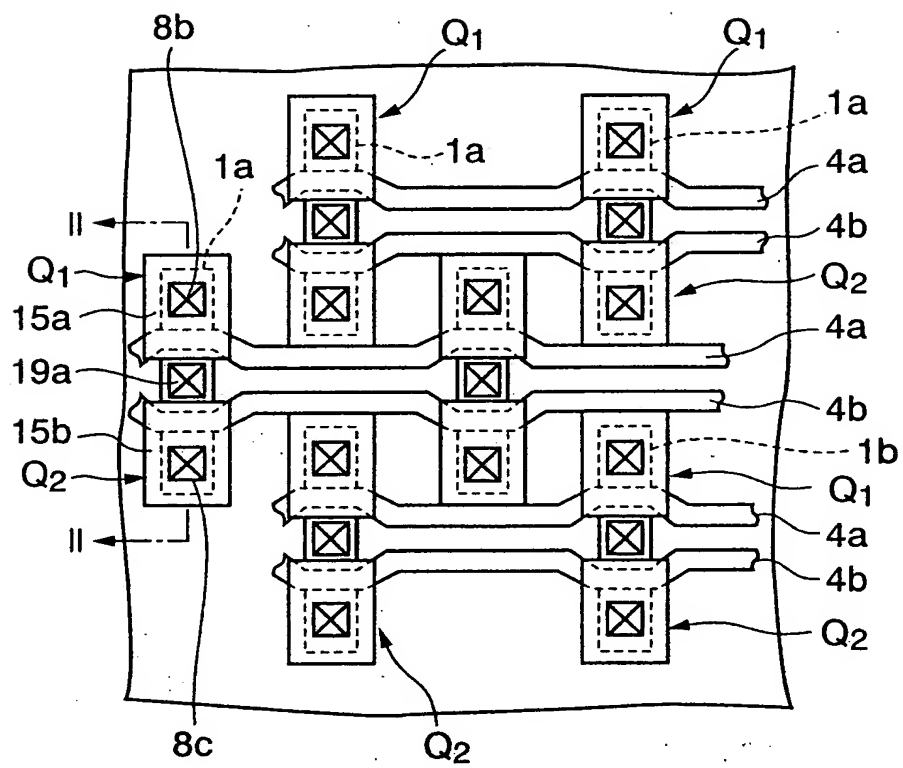


FIG. 5A

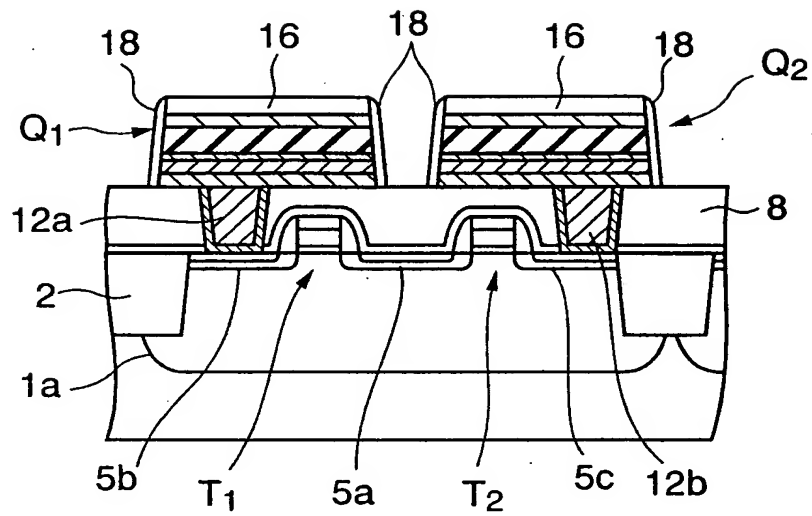


FIG. 5B

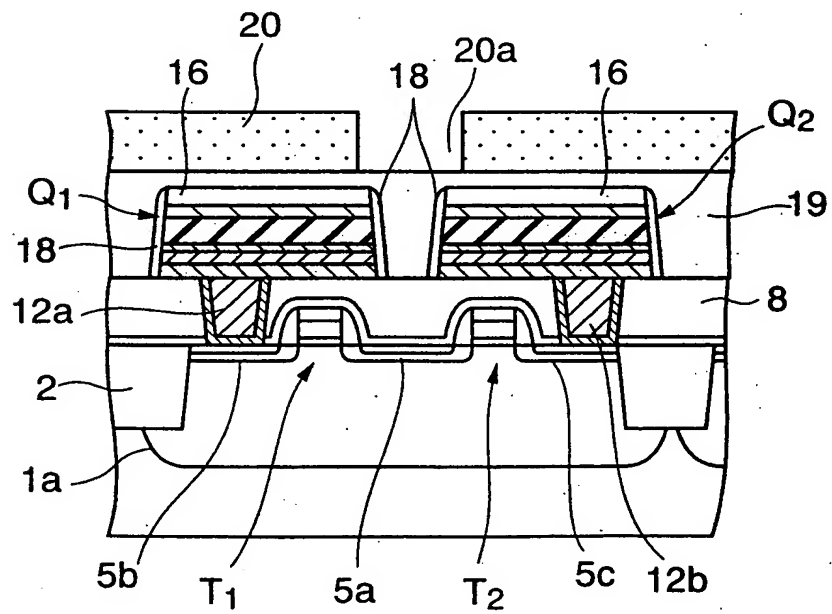


FIG. 5C

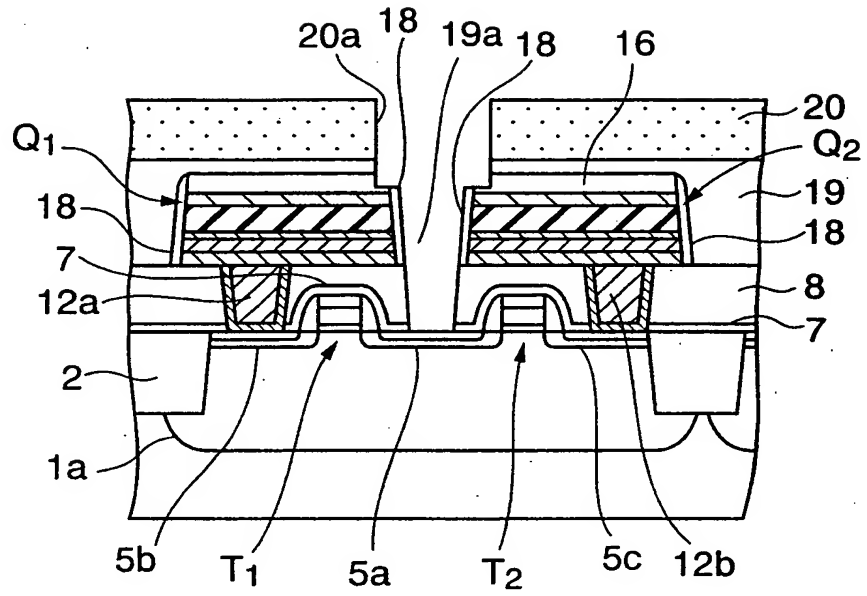


FIG. 5D.

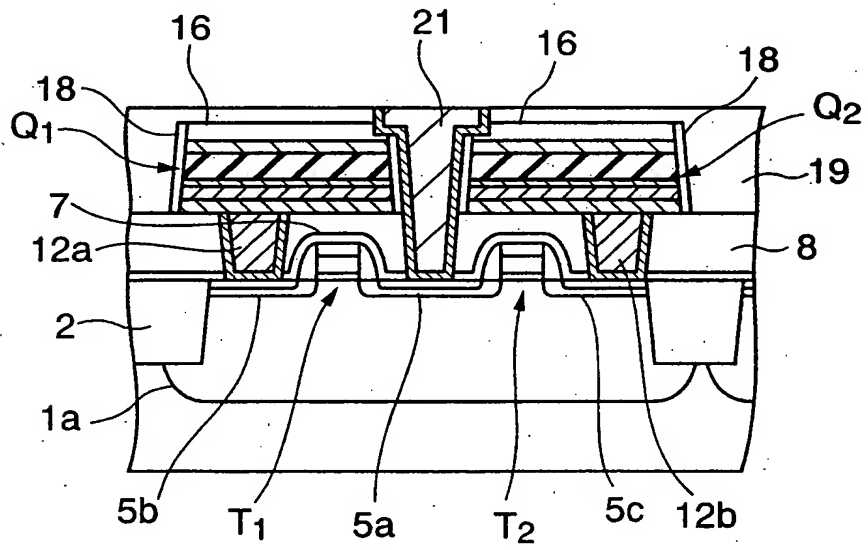


FIG. 5E

